

CLAIMS

What is claimed is:

1. A signal peak detect circuit comprises:
 - 5 an input coupling circuit operably couple to receive a signal and to convert the signal into a first input and a rectifying input; and
 - a rectifying operation amplifier including:
 - 10 first input transistor operably coupled to receive the first input;
 - second input transistor;
 - rectifying transistor operably coupled to receive the rectifying input;
 - 15 current source operably coupled to provide a reference current to the first input transistor, second input transistor, and the rectifying transistor;
 - first active input load transistor operably coupled to provide a first active load for the first input transistor and the rectifying transistor;
 - 20 second active input load transistor operably coupled to provide a second active load for the second transistor;
 - active output load transistor operably coupled to mirror the reference current; and
 - output transconductance stage operably coupled to the active load transistor and to the first input transistor and the rectifying transistor, wherein the output transconductance stage provides a rectified output representing a peak value of
 - 25 the signal.
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2. The signal peak detector of claim 1 further comprises:

a low pass filter operably coupled to the output of the output transconductance stage.

5 3. The signal peak detector of claim 1, wherein the signal is a single-ended signal and wherein the input coupling circuit further comprises:

AC ground circuit operably coupled to provide an AC ground, wherein the AC ground is provided to the rectifying transistor as the rectifying input; and

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filtering circuit operably coupled to filter the single-ended signal to produce a filtered single-ended signal, wherein the filtering circuit provides the filtered single-ended signal to the first input transistor as the first input, wherein the output transconductance stage provides a half wave rectified output representing the peak value of the signal.

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4. The signal peak detector of claim 3, wherein the filtering circuit further comprises:

first capacitor operably coupled to receive the single-ended signal;

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resistor having a first node and a second node, wherein the first node of the resistor is coupled to the first capacitor and second node of the resistor is coupled to the AC ground; and

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a second capacitor operably coupled to the first node of the resistor and to a DC ground, wherein the first and second capacitors scale the single-ended signal.

5. The signal peak detector of claim 1, wherein the signal is a differential signal and wherein the input coupling circuit further comprises:

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5 differential filtering circuit operably coupled to filter the differential signal to produce a filtered differential signal, wherein a positive leg of the filtered differential signal is provided as the first input and a negative leg of the filtered differential signal is provided as the rectifying input, wherein the output transconductance stage provides a full wave rectified output representing the peak value of the signal.

6. The signal peak detector of claim 5, wherein the differential filtering circuit further comprises:

10 first input capacitor operably coupled to receive a positive leg of the differential signal;

second input capacitor operably coupled to receive a negative leg of the differential signal;

15 first resistor having a first node and a second node, wherein the first node of the first resistor is coupled to the first input capacitor;

second resistor having a first node and a second node, wherein the first node of the second resistor is coupled to the second capacitor, and wherein the second nodes of the
20 first and second resistors are coupled together; and

common mode capacitor operably coupled to the first nodes of the first and second capacitors.

25 7. The signal peak detector of claim 1 further comprises:

the first input transistor, the second input transistor, and the rectifying transistor are implemented as PMOS transistors; and

30 the first and second active input load transistors are implemented as NMOS transistors.

8. The signal peak detector of claim 1 further comprises:

the first input transistor, the second input transistor, and the rectifying transistor are implemented as NMOS transistors; and

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the first and second active input load transistors are implemented as PMOS transistors.

9. A rectifying operational amplifier comprises:

first input transistor operably coupled to receive the first input;

5 second input transistor;

rectifying transistor operably coupled to receive the rectifying input;

current source operably coupled to provide a reference current to the first input transistor,
10 second input transistor, and the rectifying transistor;

first active input load transistor operably coupled to provide a first active load for the first
input transistor and the rectifying transistor;

15 second active input load transistor operably coupled to provide a second active load for
the second transistor;

active output load transistor operably coupled to mirror the reference current; and

20 output transconductance stage operably coupled to the active load transistor and to the
first input transistor and the rectifying transistor, wherein the output transconductance
stage provides a rectified output representing a peak value of the signal.

10. The rectifying amplifier of claim 9 further comprises:

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the first input transistor, the second input transistor, and the rectifying transistor are
implemented as PMOS transistors; and

the first and second active input load transistors are implemented as NMOS transistors.

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11. The rectifying amplifier of claim 9 further comprises:

the first input transistor, the second input transistor, and the rectifying transistor are implemented as NMOS transistors; and

- 5 the first and second active input load transistors are implemented as PMOS transistors.

12. A radio frequency integrated circuit comprises:

a receiver section operably coupled to convert inbound radio frequency signals into inbound intermediate frequency signals;

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transmitter section operably coupled to convert outbound intermediate frequency signals into outbound radio frequency signals; and

transmit/receive switch operably coupled to connect either the receiver section or the
10 transmitter section to an antenna, wherein the transmitter section includes:

mixing module operably coupled to convert the outbound low intermediate frequency signal into a radio frequency signal;

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power amplifier operably coupled to amplify the radio frequency signal to produce an amplified radio frequency signal;

bandpass filter operably coupled to filter the amplified radio frequency signal to produce the outbound radio frequency signal; and

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transmit signal strength indication module operably coupled to monitor transmit power of the power amplifier, the bandpass filter, or the transmit/receive switch, wherein the transmit signal strength indication module includes a peak detection circuit and a peak to power conversion module, wherein the peak detection circuit
25 includes:

an input coupling circuit operably couple to receive the amplified radio frequency signal, the outbound radio frequency signal, or a transmit radio frequency signal as an input signal and to convert the input signal into a first input and a rectifying input; and

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a rectifying operation amplifier including:

first input transistor operably coupled to receive the first input;

5 second input transistor;

rectifying transistor operably coupled to receive the rectifying input;

10 current source operably coupled to provide a reference current to the first input transistor, second input transistor, and the rectifying transistor;

15 first active input load transistor operably coupled to provide a first active load for the first input transistor and the rectifying transistor;

second active input load transistor operably coupled to provide a second active load for the second transistor;

20 active output load transistor operably coupled to mirror the reference current; and

25 output transconductance stage operably coupled to the active load transistor and to the first input transistor and the rectifying transistor, wherein the output transconductance stage provides a rectified output representing a peak value of the signal.

13. The radio frequency integrated circuit of claim 12, wherein the peak detection circuit further comprises:

30 a low pass filter operably coupled to the output of the output transconductance stage.

14. The radio frequency integrated circuit of claim 12, wherein the input signal is a single-ended signal and wherein the input coupling circuit further comprises:

- 5 AC ground circuit operably coupled to provide an AC ground, wherein the AC ground is provided to the rectifying transistor as the rectifying input; and

filtering circuit operably coupled to filter the single-ended signal to produce a filtered single-ended signal, wherein the filtering circuit provides the filtered single-ended signal
10 to the first input transistor as the first input, wherein the output transconductance stage provides a half wave rectified output representing the peak value of the input signal.

15 15. The radio frequency integrated circuit of claim 14, wherein the filtering circuit further comprises:

first capacitor operably coupled to receive the single-ended signal;

resistor having a first node and a second node, wherein the first node of the resistor is coupled to the first capacitor and second node of the resistor is coupled to the AC ground;
20 and

a second capacitor operably coupled to the first node of the resistor and to a DC ground, wherein the first and second capacitors scale the single-ended signal.

- 25 16. The radio frequency integrated circuit of claim 12, wherein the input signal is a differential signal and wherein the input coupling circuit further comprises:

differential filtering circuit operably coupled to filter the differential signal to produce a filtered differential signal, wherein a positive leg of the filtered differential signal is
30 provided as the first input and a negative leg of the filtered differential signal is provided

as the rectifying input, wherein the output transconductance stage provides a full wave rectified output representing the peak value of the input signal.

17. The radio frequency integrated circuit of claim 16, wherein the differential
5 filtering circuit further comprises:

first input capacitor operably coupled to receive a positive leg of the differential signal;

10 second input capacitor operably coupled to receive a negative leg of the differential signal;

first resistor having a first node and a second node, wherein the first node of the first resistor is coupled to the first input capacitor;

- 15 second resistor having a first node and a second node, wherein the first node of the second resistor is coupled to the second capacitor, and wherein the second nodes of the first and second resistors are coupled together; and

20 common mode capacitor operably coupled to the first nodes of the first and second capacitors.

18. The radio frequency integrated circuit of claim 12 further comprises:

25 the first input transistor, the second input transistor, and the rectifying transistor are implemented as PMOS transistors; and

the first and second active input load transistors are implemented as NMOS transistors.

19. The radio frequency integrated circuit of claim 12 further comprises:
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the first input transistor, the second input transistor, and the rectifying transistor are implemented as NMOS transistors; and

the first and second active input load transistors are implemented as PMOS transistors.